SN-MCB

SPI to BiSS-C Interface IC with RS-422-Style Differential Line I/O

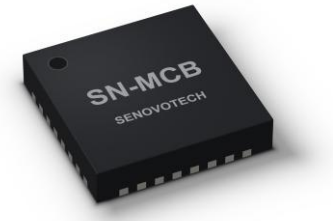
SN-MCB is an application-specific interface IC that adds a standard BiSS-C output to a sensor MCU that already has angle data. The MCU, acting as SPI master, writes position and status flags frame by frame into an on-chip buffer. When the BiSS master clocks MA, the device outputs a complete BiSS-C frame. Master reads are handled entirely by the device, with no MCU response required.

Features

- SPI slave: mode 0 / mode 3, 8-bit, MSB first, up to 10 MHz (target)
- 6-byte position write frame, optional 7-byte frame with CRC-8
- Writes take effect as a whole frame on NCS rising edge; invalid frames are discarded and the previous value is kept
- Upper 4 status bits are fixed, allowing MISO fault detection
- Glitch filtering on NCS and MA inputs
- BiSS-C single-channel slave, 1–32-bit resolution, MA up to 10 MHz (target)
- RS-422-style differential line I/O, **3.3 V levels only**
- nERR and nWRN written by the MCU, output in each frame and covered by CRC6
- Adaptive timeout by default, or fixed 1–500 µs
- Non-volatile configuration, loaded automatically at power-up
- VDD 3.135–3.465 V, −40 to +85 °C operating temperature, QFN32 package

Applications

- Absolute rotary and linear encoders
- Robot joint position feedback
- Servo motor position feedback
- Adding a BiSS-C interface to existing sensor MCUs



QFN32 package (illustration)

Preliminary: This is a preliminary document. Stated performance is target specification, is not guaranteed, and may change before final release. The pin assignment may change in production devices. Parameters marked TBD will be added in a later revision.

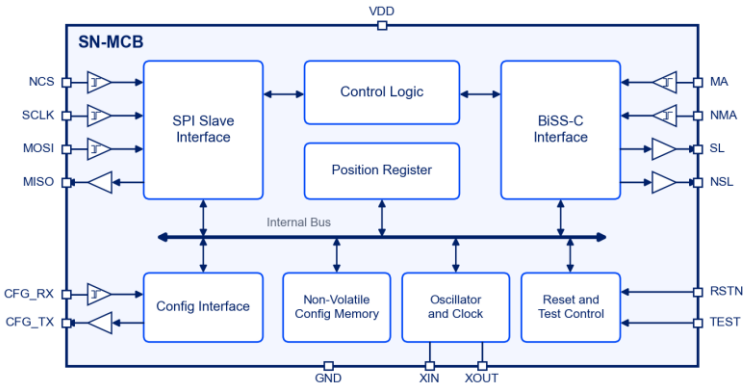


Figure 1 SN-MCB functional block diagram

Revision History

Version	Date	Changes
V0.32	2026-11-11	Preliminary release; specifications and usage notes refined

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1 Product Overview

1.1 Principle of Operation

The customer MCU writes the latest position and the nERR and nWRN flags to SN-MCB over SPI. Once a write frame passes validation on NCS rising edge, position and flags are updated in the position buffer at the same time. When the BiSS master starts a read, the device latches the data from the buffer on the first MA rising edge and shifts it out bit by bit on the MA clock.

Writes and reads are independent. An SPI write during frame transmission does not affect the frame being output; the new value takes effect from the next frame.

1.2 Device Identification

The MCU can read the device ID with the `0x90` command to confirm device type and version. The ID for this datasheet is `53 4E 01 10`. See section 5.5 for the meaning of each byte.

2 Pins

2.1 Pin Assignment

> **Note:** The pin assignment may change in production devices, and the NMA and NSL pin numbers are to be determined. Confirm the latest pin definition with SENOVOTECH before finalizing a PCB.

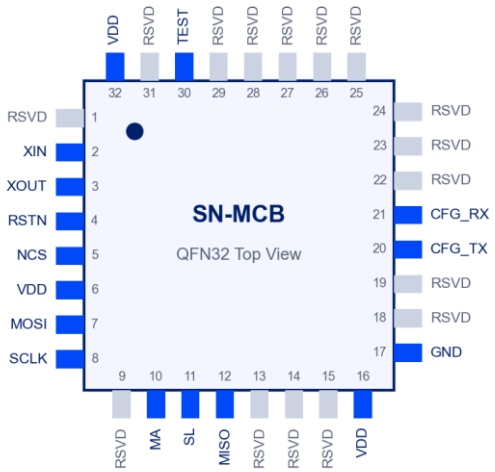


Figure 2 QFN32 pin assignment (top view)

2.2 Pin Functions

Table 1 Pin functions

Pin	Name	Type	Description
2, 3	XIN, XOUT	Analog	External 8 MHz passive crystal
4	RSTN	Input	Reset, active low, internal pull-up
5	NCS	Input	SPI chip select, active low. Internal weak pull-up, 40 kΩ typical
6, 16, 32	VDD	Power	Supply, 3.3 V; connect all three pins
7	MOSI	Input	SPI data input

Pin	Name	Type	Description
8	SCLK	Input	SPI clock
10	MA	Input	BiSS clock input, 3.3 V level. Internal weak pull-up, 40 kΩ typical
11	SL	Output	BiSS data output, 3.3 V level
TBD	NMA	Input	Inverted BiSS clock input, 3.3 V level, complementary to MA
TBD	NSL	Output	Inverted BiSS data output, 3.3 V level, complementary to SL
12	MISO	Output	SPI data output. Remains driven while NCS is high; does not go high-impedance
17	GND	Ground	Power ground
20	CFG_TX	Output	Configuration UART transmit, 3.3 V level
21	CFG_RX	Input	Configuration UART receive, 3.3 V level
30	TEST	Input	Test pin; must be connected to ground through a resistor in normal operation
1, 9, 13, 14, 15, 18, 19, 22–29, 31	RSVD	—	Reserved, do not connect

3 Electrical Characteristics

Note: Parameters marked TBD will be added in a later revision; do not assume their values in a design. SN-MCB pins are not 5 V tolerant. Input voltage must not exceed the maximum in Table 2.

3.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	−0.3	3.6	V
Pin input voltage	VIN	−0.3	3.6	V
Current per pin	IIO	—	20	mA
Storage temperature	TSTG	−40	+125	°C
Electrostatic discharge (human body model)	VESD(HBM)	—	±2	kV

3.2 Recommended Operating Conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	3.135	3.3	3.465	V
Operating ambient temperature	TA	−40	—	+85	°C
External crystal frequency	fXTAL	—	8	—	MHz

3.3 DC Characteristics

Table 4 DC characteristics (VDD = 3.3 V)

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (estimated)	IDD	—	40	—	mA
Input high level	VIH	2.0	—	—	V
Input low level	VIL	—	—	0.8	V
Output high level	VOH	2.4	—	—	V
Output low level	VOL	—	—	0.4	V
Internal pull-up resistance	RPU	—	40	—	kΩ

3.4 SPI Timing

Table 5 SPI timing

Parameter	Symbol	Min	Max	Unit
SCLK frequency, write	fSCLK	—	10	MHz
SCLK frequency, readback, no master sampling delay	fSCLK	—	7	MHz
SCLK frequency, readback, master samples about 25 ns late	fSCLK	—	10	MHz
NCS falling edge to first SCLK rising edge	tLEAD	50	—	ns
Last SCLK rising edge to NCS rising edge	tLAG	10	—	ns
NCS high time (frame gap), 250 ns or more recommended	tNCSH	~50	—	ns
MOSI setup time (to SCLK rising edge)	tSU	5	—	ns
MOSI hold time (from SCLK rising edge)	tH	15	—	ns
SCLK falling edge to MISO valid	tDO	—	40	ns

Frequencies in Table 5 and Table 6 are target specifications. Other timing values are design values. None of these values are guaranteed.

3.5 BiSS Timing

Table 6 BiSS timing

Parameter	Symbol	Min	Max	Unit
MA clock frequency (target)	fMA	See 6.3	10	MHz
MA high time	tMAH	~20	—	ns
MA low time	tMAL	~20	—	ns
MA rising edge to SL update	tMS	—	60	ns
Power-up to internal initialization complete; READY is set afterwards	tINIT	—	40	ms

4 Functional Description

4.1 Power-Up Behavior

After power-up the device loads its configuration from non-volatile memory, then sets the READY bit in the status byte. The behavior at each stage is shown below.

Table 7 Behavior during power-up

Stage	SPI	BiSS output
Before internal initialization completes	Not available	Pins are high-impedance for up to 40 ms. Add external pull-up or pull-down resistors if the power-up level matters
READY = 0	Accessible	SL held high, MA ignored
READY = 1, no position written yet	Accessible	Frames output normally with POS = 0, nERR = nWRN = 0 (indicating error)
Position written	Accessible	Latest written position and flags output normally

4.2 Position Buffer

- The buffer is one level deep, with no FIFO. The master always reads the last valid written value.
- Position and flags are updated at the same instant, so the master never reads a mix of old and new data.
- The first MA rising edge latches position, flags and the current resolution together. All three stay constant within a frame.
- If no new write occurs between two master reads, the master reads the same value again.

Note: POS_VALID stays at 1 after the first valid write and does not indicate whether data is fresh. This version has no policy for handling the absence of new data. When sensor data is invalid, the MCU should write nERR = 0 and let the master decide.

5 SPI Interface

5.1 Interface Parameters

Table 8 SPI interface parameters

Item	Specification
Role	Slave
Mode	Mode 0 or mode 3, determined by the idle SCLK level; no configuration needed
Word length and bit order	8-bit, MSB first
Sampling and update	MOSI sampled on rising edge, MISO updated on falling edge
Frame delimiting	A frame starts immediately on NCS falling edge. It ends once NCS has been high and stable for about 50 ns; writes take effect at that point
Write clock	Up to 10 MHz (target), mode 0 and mode 3
Readback clock	Direct read at 7 MHz and below. At 8 MHz and above the master must delay its MISO sampling point by about 25 ns

Note: MISO remains driven while NCS is high. In this version MISO cannot be shared with other SPI slaves.

Note: A high level on NCS shorter than about 50 ns is treated as a glitch and does not end the current frame. The high time between frames must not be shorter than about 50 ns; 250 ns or more is recommended.

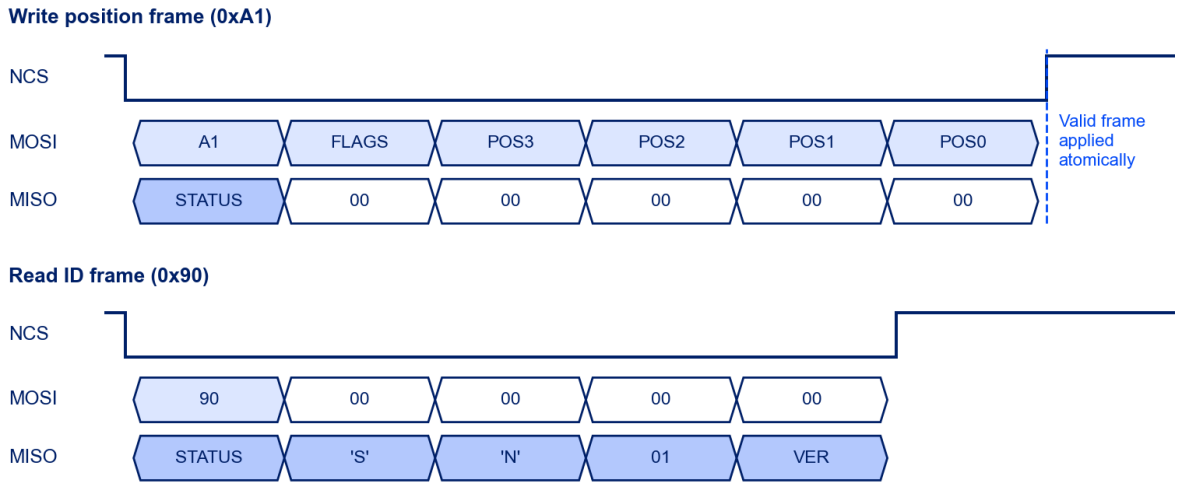


Figure 3 SPI frame structure

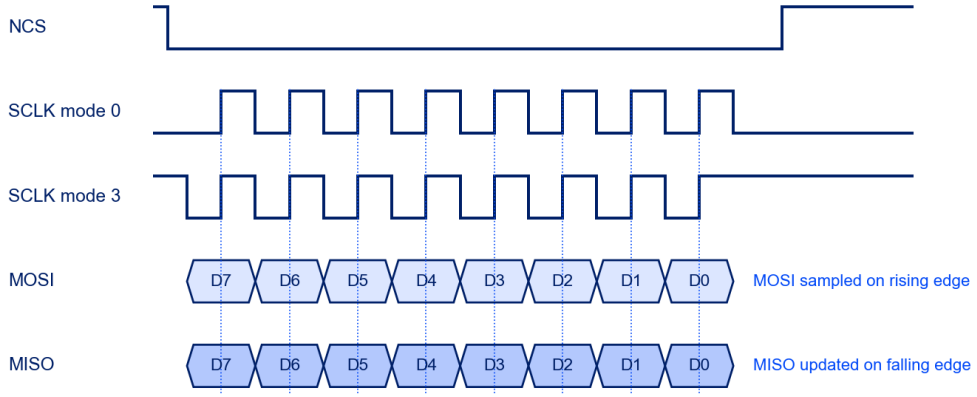


Figure 4 SPI bit timing (mode 0 and mode 3)

5.2 Command Set

The first byte of each frame is the command. While the MCU sends the command byte, MISO returns the status byte.

Table 9 SPI commands

Command	Frame content (MOSI)	Bytes	Function
0xA1	A1 FLAGS POS3 POS2 POS1 POS0	6	Write position
0xB1	B1 FLAGS POS3 POS2 POS1 POS0 CRC8	7	Write position with CRC-8
0x90	90 + 4 arbitrary bytes	Up to 5	Read device ID
0x91	91 + 3 arbitrary bytes	Up to 4	Read current configuration
0x9F	9F	1 or more	Read status byte only

5.3 Status Byte

The status byte is captured on NCS falling edge and reflects the state at the start of the frame.

Table 10 Status byte

Bit	Name	Meaning
7:4	Fixed	Always `0101`. Any other value indicates a MISO connection or timing fault
3	POS_VALID	1 = a valid position write has occurred since reset
2	BISS_BUSY	1 = a BiSS frame is in progress, including the timeout phase
1	SPI_ERR	1 = the previous frame was judged an error; cleared after the next valid frame ends
0	READY	1 = configuration complete, BiSS output enabled

5.4 Position Write

Table 11 Position write frame fields

Field	Description
FLAGS	Bit 0 is nERR, bit 1 is nWRN; 1 means no error or no warning. Other bits are ignored; writing 0 is recommended
POS3…POS0	32-bit position, big-endian, right-aligned. Only the low N bits are sent (N is the configured resolution); upper bits are ignored
CRC8	`0xB1` frames only, see the table below

Table 12 CRC-8 parameters

Item	Specification
Polynomial	$x^8 + x^2 + x + 1$ (`0x07`)
Initial value	`0x00`
Final XOR	None
Bit order	MSB first, not reflected
Coverage	First 6 bytes of the frame, including command byte `0xB1`

Example: writing POS = 443964 (`0x0006C63C`) with nERR = nWRN = 1 gives the complete frame `B1 03 00 06 C6 3C 9C`.

5.5 Read Commands

A read frame may end early on any byte boundary. Bytes beyond the defined length return `0x00`.

Table 13 Read command data

Command	Byte	Content
`0x90`	1	`0x53` (ASCII S)
	2	`0x4E` (ASCII N)
	3	Product series code, `0x01` for this product
	4	Version: upper 4 bits major, lower 4 bits minor. `0x10` (1.0) for this version
`0x91`	1	Resolution N (1–32)
	2, 3	BiSS timeout, high byte first, in units of 10 ns. 0 means adaptive

With the factory default configuration, `0x91` returns `13 00 00`, that is 19 bits and adaptive timeout.

5.6 Error Handling

Table 14 SPI frame evaluation

Condition at NCS rising edge	Position buffer	SPI_ERR bit
Write frame with correct byte count, validation passed	Updated	Cleared
Read frame of a whole number of bytes	Unchanged	Cleared
Write frame with too many or too few bytes	Unchanged	Set
`0xB1` frame with CRC-8 error	Unchanged	Set
Frame does not end on a byte boundary	Unchanged	Set
Unknown command	Unchanged	Set
NCS low with no clock (not counted as a frame)	Unchanged	Keeps previous value

5.7 Reference Code

```
/* spi_xfer() is user-supplied: drive NCS low, transfer n bytes full duplex, drive NCS high */
void spi_xfer(const uint8_t *tx, uint8_t *rx, unsigned n);

static uint8_t sn_crc8(const uint8_t *d, unsigned n)
{
    uint8_t c = 0;
    while (n--) {
        c ^= *d++;
        for (int i = 0; i < 8; i++)
            c = (c & 0x80) ? (uint8_t)((c << 1) ^ 0x07) : (uint8_t)(c << 1);
    }
    return c;
}

/* Write position; returns the status byte (reflects the result of the previous frame) */
uint8_t sn_write_pos(uint32_t pos, uint8_t n_err, uint8_t n_wrn)
{
    uint8_t tx[7], rx[7];
    tx[0] = 0xB1;
    tx[1] = (uint8_t)((n_err & 1u) | ((n_wrn & 1u) << 1));
    tx[2] = (uint8_t)(pos >> 24);
    tx[3] = (uint8_t)(pos >> 16);
    tx[4] = (uint8_t)(pos >> 8);
    tx[5] = (uint8_t)pos;
    tx[6] = sn_crc8(tx, 6);
    spi_xfer(tx, rx, 7);
    return rx[0];
}
```

6 BiSS-C Interface

6.1 Frame Structure

SN-MCB outputs single-channel BiSS-C frames. MA idles high, and one bit is output per rising edge. Reading a complete frame takes N + 12 MA rising edges, where N is the configured resolution. MA high and low times must each be at least about 20 ns; shorter pulses are ignored by the input filter.

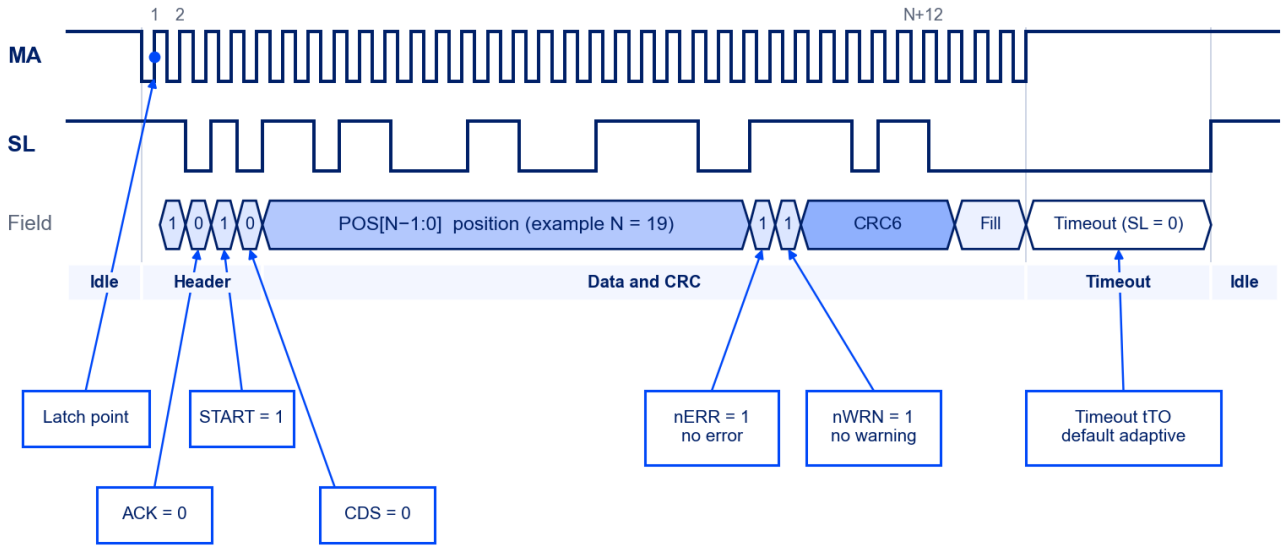


Figure 5 BiSS-C frame timing (example: N = 19, master issues 4 extra clocks)

Table 15 BiSS-C frame fields

Rising edge	Field	Bits	Description
1	Lead-in	1	Always 1; position is latched at this edge
2	ACK	1	Always 0
3	START	1	Always 1
4	CDS	1	Always 0; register communication is not supported in this version
5…	POS[N−1:0]	N	Position, MSB first
N+5	nERR	1	From FLAGS bit 0
N+6	nWRN	1	From FLAGS bit 1
N+7…N+12	CRC6	6	Inverted CRC is transmitted, MSB first
After	Fill	—	Outputs 0 while clocking continues

6.2 CRC6

Table 16 CRC6 parameters

Item	Specification
Polynomial	$x^6 + x + 1$ (0x43)
Initial value	0
Coverage	POS MSB through nWRN, MSB first
Transmission	Inverted before transmission

Example: with N = 19, POS = 443964 and nERR = nWRN = 1, SL outputs the following (left to right: lead-in and header bits up to CDS, POS, nERR and nWRN, CRC6):

```
1010  1101100011000111100  11  110110
```

6.3 Timeout

After the last rising edge MA stays high. Once the timeout elapses the frame ends, SL returns high and the device can accept the next frame.

Table 17 Timeout modes

Mode	Timeout	Suitable for
Fixed	Configurable from 1–500 µs	Systems where MA frequency is known or varies widely
Adaptive (default)	Measured each frame: 1.5 MA periods plus about 120 ns	Systems with a stable MA frequency that want a shorter frame gap

- The high time of every MA period must be shorter than the timeout, otherwise the frame ends early.
- Between frames the master should hold MA high for at least the timeout.
- In the default adaptive mode the timeout follows the MA frequency. If the MA line is noisy, use `SET:TIMEOUT=20` to select a fixed 20 µs timeout.
- If the master issues extra clocks after the CRC, SL outputs 0 and stays low during the timeout (see Figure 5). If there are no further MA rising edges after the last CRC bit, SL holds the level of the last bit until it returns high when the timeout ends.
- Adaptive mode needs at least two MA rising edges to complete its measurement. Glitches shorter than about 20 ns are filtered out, but wider isolated pulses can still misalign the next frame. The master should detect this with CRC6, and a fixed timeout is recommended in noisy environments.

6.4 Line Interface

SN-MCB provides an RS-422-style differential line interface: MA and NMA, and SL and NSL, are complementary signals, and NSL is always the inverse of SL. **This interface supports 3.3 V CMOS levels only.** Choose a connection method from the table below.

Table 18 BiSS line connection methods

Connection	Wiring	Suitable for
3.3 V differential direct	MA, NMA, SL and NSL connected directly to the far end	On-board or short-distance links with a common ground and a 3.3 V far end
External RS-422 transceiver	MA and SL connected to the transceiver; NMA and NSL left unconnected	BiSS cables and any other line requiring RS-422 levels

Note: These four pins support 3.3 V levels only and do not themselves meet the RS-422 electrical specification. They do not tolerate line common-mode voltage. Input voltage must not exceed the maximum in Table 2. An external transceiver is required to connect to an RS-422 line. Do not drive a 100 Ω line termination directly from SL or NSL. Current per pin must not exceed the limit in Table 2.

7 Configuration

7.1 Configuration UART

Resolution and timeout are set through the configuration UART: 115200 baud, 8 data bits, no parity, 1 stop bit, 3.3 V level. Each command ends with `\n`; `\r` is ignored. The maximum line length is 31 characters.

Table 19 UART commands

Command	Function	Response on success
`INFO?`	Read current status	Status line
`SET:BITS=n`	Set resolution, n = 1–32, effective immediately	`OK`
`SET:TIMEOUT=n`	Set timeout, n in µs, range 0–500, 0 means adaptive, effective immediately	`OK`
`SAVE`	Write the current configuration to non-volatile memory	`OK`
`TEST:ON`	Enable test mode	`OK`
`TEST:OFF`	Disable test mode	`OK`

On error the device returns a line of text beginning with `ERR:`. The `INFO?` response is a single line, for example:

```
SN-MCB,SERIES=1,VER=1.0,BITS=19,TIMEOUT=0,POSVALID=1,FRAMES=12,SPI_OK=25,SPI_ERR=0,POS=443964,FLAGS=3,TEST=0
```

Table 20 INFO? fields

Field	Meaning
BITS / TIMEOUT	Resolution / timeout (µs, 0 = adaptive)
POSVALID	POS_VALID in the status byte
FRAMES	Count of latched BiSS frames
SPI_OK / SPI_ERR	Count of valid write frames / error frames
POS / FLAGS	Position / flags currently in the buffer (bit 0 nERR, bit 1 nWRN)
TEST	Test mode state

7.2 Saving the Configuration

- `SET` commands change only the running configuration, which is lost at power-off. Send `SAVE` to keep it.
- If the stored configuration is invalid at power-up, the device uses the defaults: 19 bits, adaptive timeout.
- `SAVE` is rated for at least 10,000 write cycles. Do not call it in a periodic task.

7.3 Configuration Tool

SENOVOTECH provides a browser-based configuration tool for connecting, viewing status, changing settings and saving. It must be opened in a browser that supports Web Serial, such as Chrome or Edge.

7.4 Test Mode

`TEST:ON` makes the device sweep the position cyclically over the configured full scale with a 10 s period, with no external MCU needed and nERR = nWRN = 1. Test mode is not saved and is off again after power-off.

> **Note:** In test mode the master reads sweep data that looks valid, with status flags showing no error. Do not enable it in a production system.

8 Application Information

8.1 Typical Connection

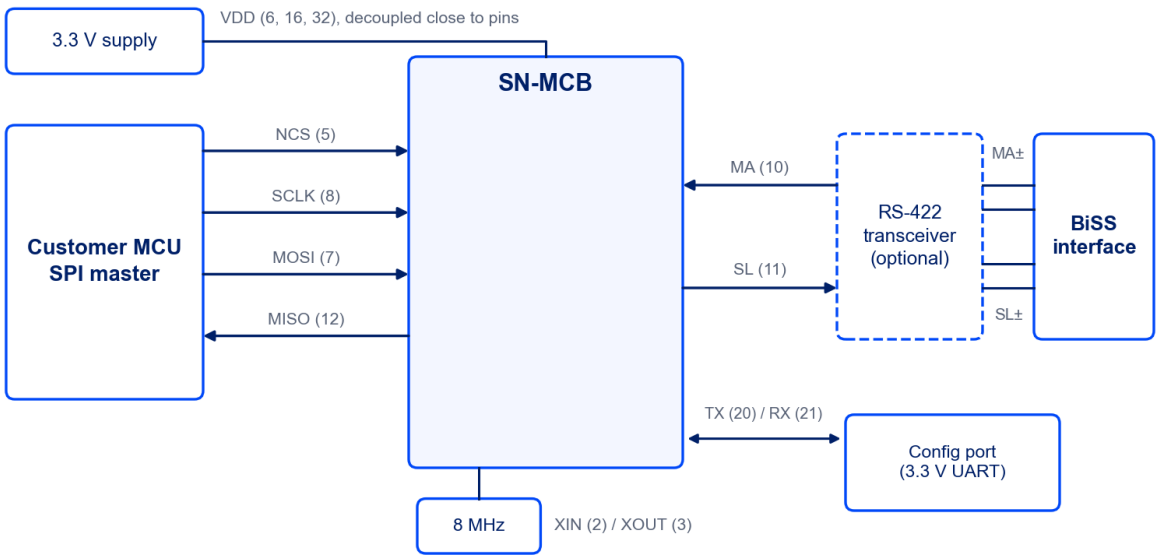


Figure 6 Typical application connection (BiSS line through external RS-422 transceiver)

- The BiSS line interface **supports 3.3 V levels only**. Add an external RS-422 transceiver when standard RS-422 levels are needed; see section 6.4 for connection methods.
- Connect an 8 MHz passive crystal to XIN and XOUT. Select load capacitors to the crystal specification and place them close to the pins.
- Place a 100 nF decoupling capacitor close to each power pin. Add a ferrite bead if the supply is noisy.
- SL and NSL are high-impedance during power-up initialization. If the master is sensitive to this, add an external pull-up on SL and a pull-down on NSL.
- Providing test points for the configuration UART is recommended for production configuration and field diagnostics.

8.2 MCU Software Flow

1. After power-up, poll the status byte (`0x9F`) until READY = 1.
2. Read the device ID (`0x90`) and configuration (`0x91`) to confirm the device and resolution are as expected.
3. Write the position periodically, preferably with `0xB1` frames. The write period should be shorter than the master read period.
4. Check the status byte returned by the next frame: the upper 4 bits should be `0101` and SPI_ERR should be 0.

9 Limitations of This Version

This version does not support: register communication (CDM / CDS), BiSS bus and daisy-chain operation, interrupt (IRQ) output, CRC16, a policy for handling the absence of new data, or sharing MISO among multiple SPI slaves.

10 Package and Ordering Information

Table 21 Ordering information

Part number	Package	Operating temperature
SN-MCB	QFN32	−40 to +85 °C

Table 22 QFN32 package dimensions (mm)

Symbol	Parameter	Min	Typ	Max
D / E	Package body size	3.90	4.00	4.10
A	Overall height	0.80	0.85	0.90
A1	Standoff	0.00	0.02	0.05
b	Lead width	0.15	0.20	0.25
e	Lead pitch	—	0.40	—
L	Lead length	0.20	0.30	0.40
D2 / E2	Exposed pad size	2.60	2.70	2.80

Exposed pad electrical connection, recommended land pattern and packing specification: TBD.

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